Cryogenic Characterization of Ferroelectric Non-volatile Capacitors

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Capacitive crossbar arrays based on ferroelectric non-volatile capacitors (nvCaps) [1] have shown strong potential for energy-efficient in-memory computing, particularly because they avoid the static power losses and sneak path issues seen in resistive arrays. However, the precision of these arrays in performing multiply-and-accumulate (MAC) operations is limited by thermal noise, which affects the effective number of bits (ENOB) [2]. Since this noise scales with temperature (see Fig. 1(a)-(b)), operating the system at cryogenic temperatures presents a natural way to improve computational accuracy. In this work, we analyzed nvCaps' operation in GlobalFoundries' 28 nm ferroelectric field effect transistor (FeFET) platform, characterizing their memory window and retention behavior at temperatures down to 77 K. We then used these insights to model and simulate full-array behavior under cryogenic conditions.

Our measurements showed that while the memory window narrows and the C-V curve shifts at 77 K (see Fig. 1(c)-(e)) due to lower carrier density [3], the devices maintain a strong on/off capacitance ratio after pulse programming (see Fig. 2(a)-(b)). More importantly, we observed significantly reduced degradation in the on-state capacitance when the devices are held under low-voltage read stress at cryogenic temperatures (see Fig. 2(c)-(d)). These improvements are consistent with reduced domain wall motion and suppressed depolarization at low temperatures. Building on this, we simulated a 128×128 capacitive crossbar array using calibrated device models and peripheral circuitry from a commercial PDK. The simulations showed that ENOB improves from about 4 bits at room temperature to 5 bits at 77 K (see Fig. 2(e)-(f)).

Together, these results highlighted the viability of nvCap-based capacitive crossbars for precision analog computing in low-temperature environments. The combination of better retention, reduced noise, and higher accuracy makes this approach especially relevant for future systems operating in cryogenic domains, such as quantum computing interfaces, aerospace electronics, and high-performance data centers.

References

[1] T.-H. Kim *et al.*, EDL 2023, [2] Y.-C. Luo *et al.*, IEDM 2024, [3] O. Phadke *et al.*, IRPS 2024

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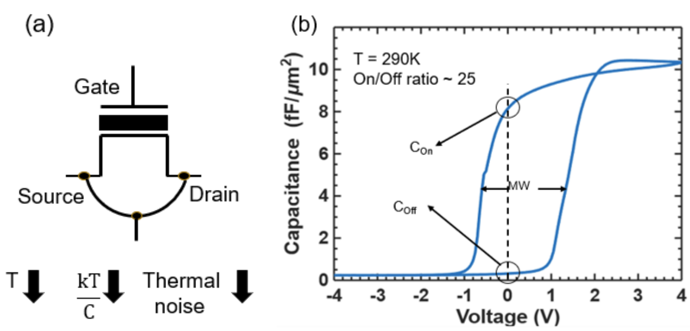
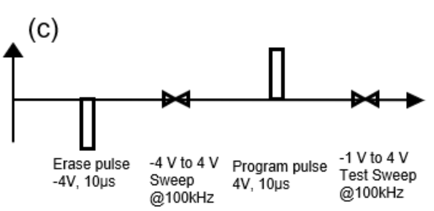




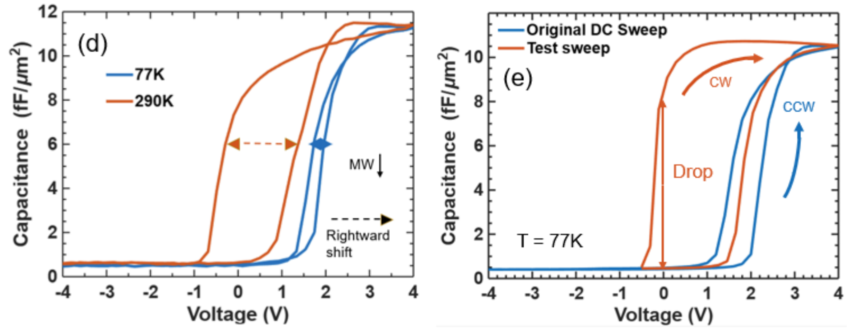
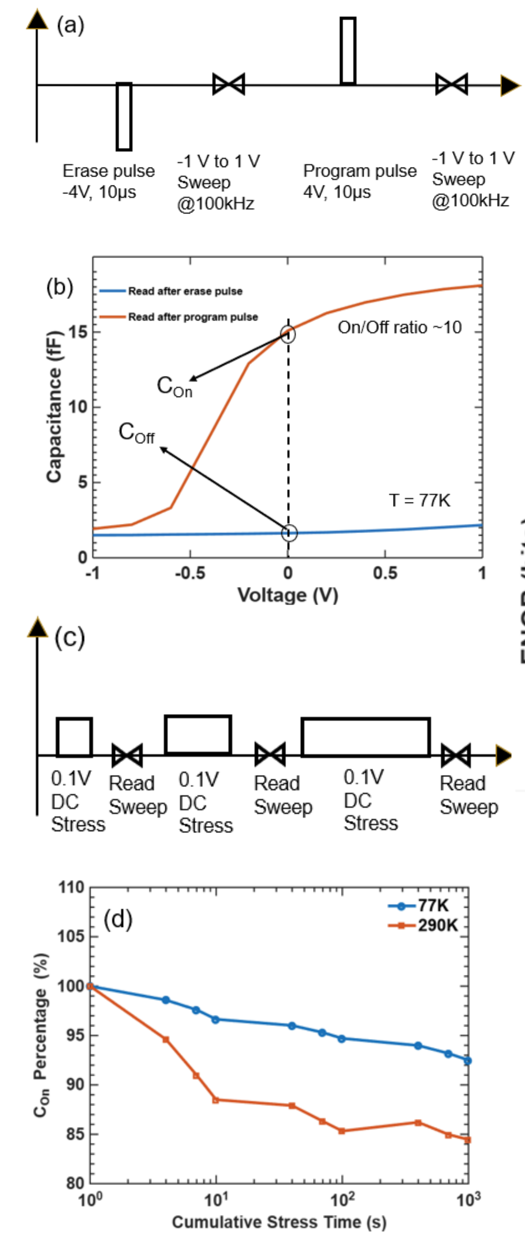


Fig 1. (a) The nvCap, (b) C-V characteristics of nvCap, (c) The pulse scheme used (d) MW shrinkage and rightward shift of the C-V curve during the quasi-static sweep at cryogenic temperatures. (e) Drop in On state capacitance after performing the test sweep confirming carrier trapping to be the mechanism behind the MW shrinkage



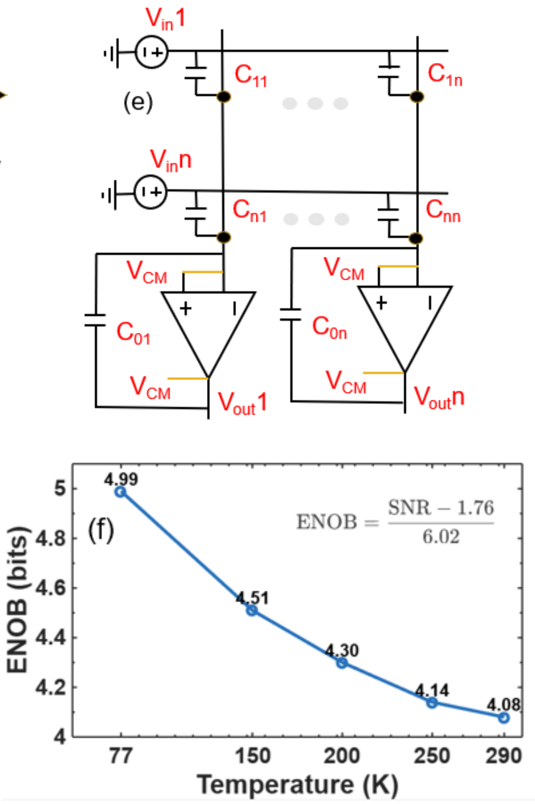


Fig 2. (a) The pulse scheme used. (b) HCS observed being programmed with a 4V, 10us pulse. (c) The pulse scheme used: 0.1V DC stress applied with read sweeps performed periodically. (d) % decay in HCS when subjected to 0.1V DC Stress. (e) The schematic of the crossbar array. (f) The ENOB versus temperature, showing ~5 bits at 77 K and ~4 bits at 290 K